

REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

Claims 1-3 and 5-40 are pending in this application. Claims 8-23 and 25-39 stand withdrawn from consideration. Claims 3 and 7 were objected to for informalities. Claims 1, 5, 24, and 40 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. patent application publication 2001/0002712 to Horiguchi et al. (herein "Horiguchi") in view of U.S. patent 6,617,639 to Wang et al. (herein "Wang"). Claims 1-3, 5, 24, and 40 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. patent 6,291,855 to Chang et al. (herein "Chang") in view of Wang. Claims 6 and 7 were objected to as dependent upon rejected base claims, but were noted as allowable if rewritten in independent form to include all of the limitations of their base claim and any intervening claims.

Applicants gratefully acknowledge the indication of allowable subject matter in claims 6 and 7.

Addressing first the objection to claims 3 and 7, those claims are amended by the present response to address the objections thereto. Specifically, claim 3 no longer recites the redundant subject matter from claim 1, and claim 7 is amended to now depend from claim 6.

Addressing now the rejection of claims 1, 5, 24, and 40 under 35 U.S.C. § 103(a) as unpatentable over Horiguchi in view of Wang, that rejection is traversed by the present response.

Initially, applicants note each of independent claims 1, 24, and 40 is amended by the present response to clarify features recited therein. Specifically, those claims clarify that the first and second control gates are formed "above the diffused layers and only on opposite sides of the floating gate." As shown for example in Figure 2A in the present specification as a non-limiting example, the control gates CG are formed above the diffused layers S/D and only on opposite sides of the floating gate FG, i.e. the first and second control gates CG are

not formed on the floating gate FG. The features clarified in the claims are believed to clearly distinguish over the applied art.

As noted above, according to claims 1, 24, and 40, first and second control gates are located above diffused layers and are formed only on opposite sides of the floating gate.

With such a claimed structure, when a film thickness of the floating gate is increased without considering any increase of a parasitic capacitance, a capacitance ratio can be secured. As a result, even when a gate length or a channel width of a cell transistor is minimized, the capacitance ratio can be increased. As the capacitance ratio can be increased, the write voltage can be reduced. Thereby, it becomes possible to simultaneously satisfy miniaturization of the cell and reduction of write voltage.¹

As noted above, the claims recite that the first and second control gates are formed only on opposite sides of the floating gate, i.e. they are not formed on the floating gate. Compared to a case in which the control gate is formed on the floating gate, the total layer thickness can be accordingly reduced. When a control gate is formed on a floating gate, which is believed to conventionally be the case, the total thickness may become so great that the floating gate and the control gate cannot be etched with high accuracy. The claimed structures allow easy etching and other kinds of treatment. Moreover, since the first and second control gates are formed above the diffused layers, the lateral sides of the cell can be similar to that in conventional art; that is the cell side does not need to be increased in the present invention. The claimed features are believed to distinguish over the applied art.

In Figure 6B Horiguchi discloses control gates 11 located above the channel region and as formed on both sides of a floating gate. However, in that structure in Horiguchi the control gates are not formed above the diffused layers 21 and 22.

¹ See for example the present specification at page 14, line 17 through page 15, line 1.

In contrast to the structure in Horiguchi, independent claims 1, 24, and 40, and the claims dependent therefrom, require that the first and second control gates are located above the diffused layer, and are formed on both sides of the floating gate. With that claimed structure the channel length can be substantially the same as the width of the floating gate, and the semiconductor device can be miniaturized. Horiguchi does not disclose such a structure. Moreover, as a result in Horiguchi the channel length is equal to the total sum of the width of the floating gate, the width of the control gates 11, and the width of the gate insulating films 15. As a result Horiguchi cannot provide miniaturization of the semiconductor devices.

Moreover, as recited in independent claims 1, 24, and 40, the first and second control gates are formed on both sides of the floating gate. With such a structure the size of the device, as viewed in the channel width direction, is substantially the same as the channel width. In contrast to that claimed structure, in Horiguchi the control gates 11 are formed around the floating gate, as shown for example in Figure 6A. With that structure the size of the device, as viewed in the channel width direction, is greater than the channel width. As a result the device of Horiguchi cannot achieve the miniaturization as in the claimed features.

In such ways, each of independent claims 1, 24, and 40 is believed to clearly distinguish over relied upon features in Horiguchi. Moreover, no teachings in Wang can cure the noted deficiencies in Horiguchi. Wang merely discloses an EEPROM that uses an ONO layer as an inter gate insulating film, but does not disclose any structure that can cure the above-notified deficiencies in Horiguchi.

In view of these foregoing comments applicants respectfully submit each of independent claims 1, 24, and 40, and the claims dependent therefrom, patentably distinguish over Horiguchi in view of Wang.

Addressing now the rejection of claims 1-3, 5, 24, and 40 under 35 U.S.C. § 103(a) as unpatentable over Chang in view of Wang, those rejections are also traversed by the present response.

The above-noted combination of teachings is also not believed to meet the features clarified in the claims.

Chang discloses, for example in Figure 5, a first conductive film 103 covered with a floating gate FG, see also column 4, lines 55-56. In Chang a third conductive film 109 is formed above the floating gate FG with a second interlevel dielectric film 107 is interposed between the floating gate FG and the film 109. As noted in Chang at column 4, line 67 to column 5, line 1, the first conductive film 103 and the third conductive film 109 constitute a control gate electrode CG.

In other words, in Chang the control gate CG is formed not only around the floating gate FG but also on the floating gate FG.

The claims set forth a different structure as in the active claims the control gate is formed above the diffused layer and only on the opposite sides of the floating gate, i.e, in the claims the control gate is not formed on the floating gate. Thus, Chang does not disclose all the features recited in the amended claims.

Moreover, Wang does not cure the deficiencies in Chang.

In view of these foregoing comments, applicants respectfully submit each of independent claims 1, 24, and 40, and the claims dependent therefrom, also distinguish over the combination of teachings of Chang in view of Wang.

In view of these foregoing comments, applicants respectfully submit each of the claims as currently written distinguishes over the applied art.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

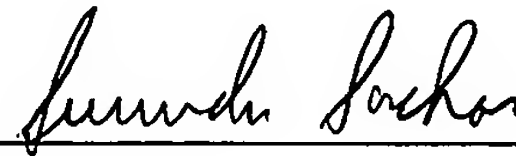
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